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(54) **Digital device for clock signal synchronization**

(57) A phase lock loop circuit for synchronizing clock signals HSYN, locally generated by a controlled oscillator 9 with respect to a received reference clock HREF comprises a digital phase comparator 1—3 for assessing the phase difference between the local clock and the reference clock and furnishing the mean value of the voltage indicative of said difference, and means 7 for storing the last instantaneous phase difference as soon as a pulse of the reference clock HREF is lost. Phase comparison of HREF and HSYN is achieved by adder 3 fed by up-counter 1 and down-counter 2. A register 7 stores the instantaneous output from adder 3. Circuitry 6 directs loss of HREF whereupon a multiplexer 8 transmits the stored value of phase difference to D-A converter 4 and oscillator 9. Up-counter 1 remains blocked after restoration of HREF until a comparison circuit 69 determines that the instantaneous and stored phase differences are equal.

FIG 5

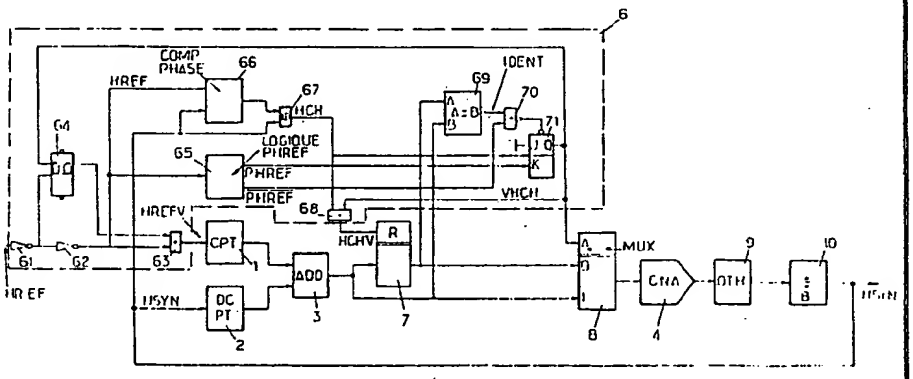

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FIG 1

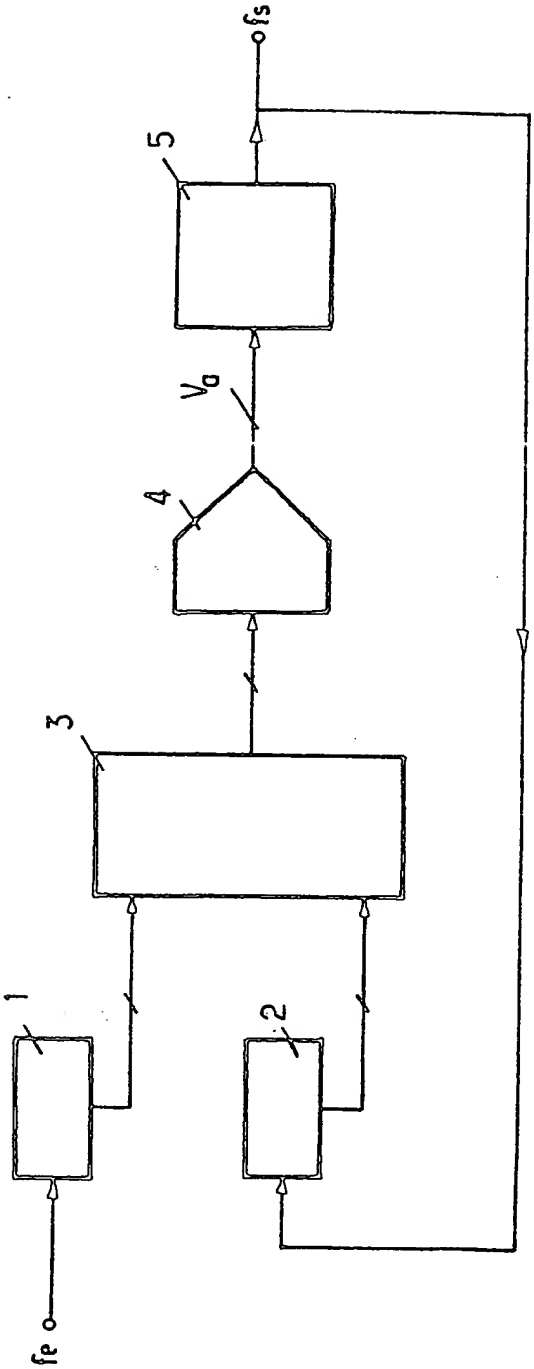
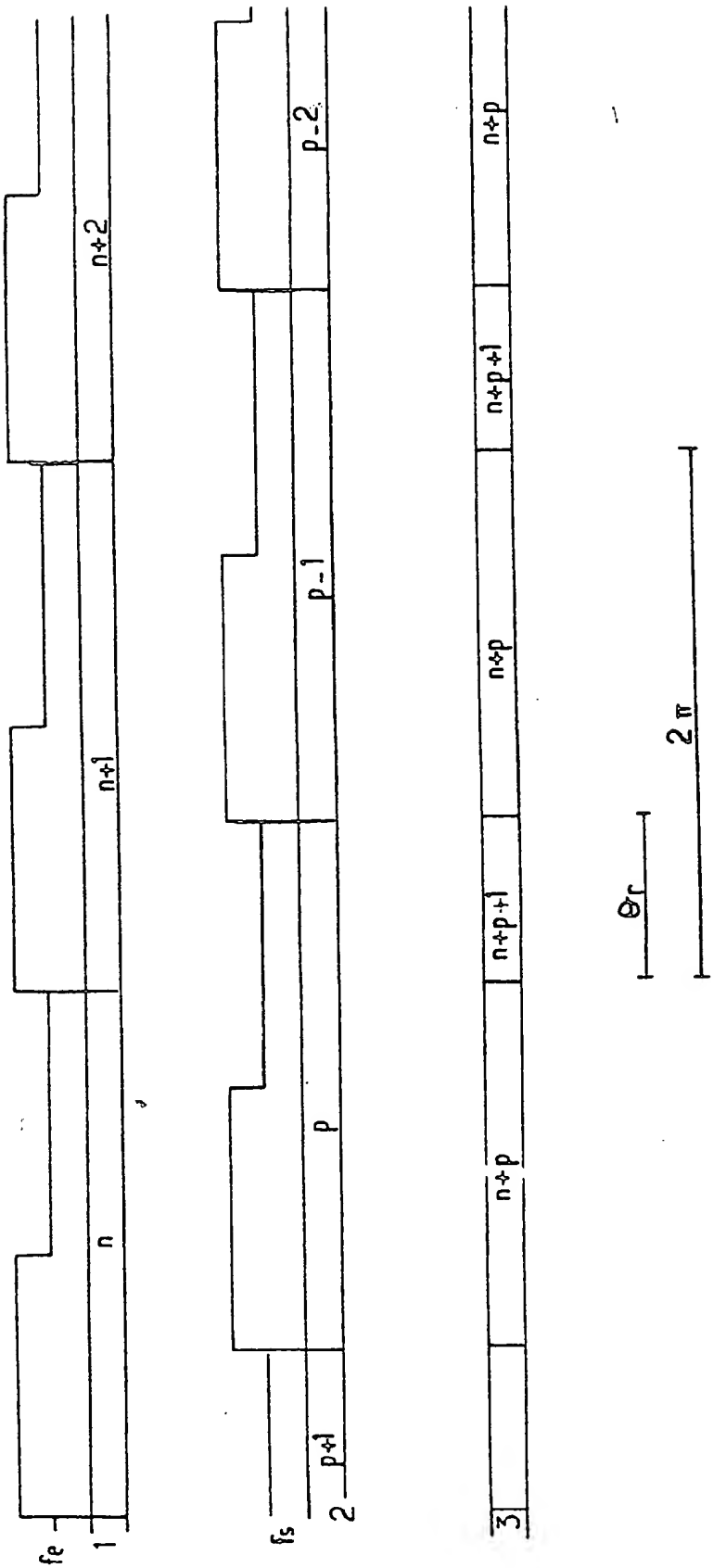


FIG 2



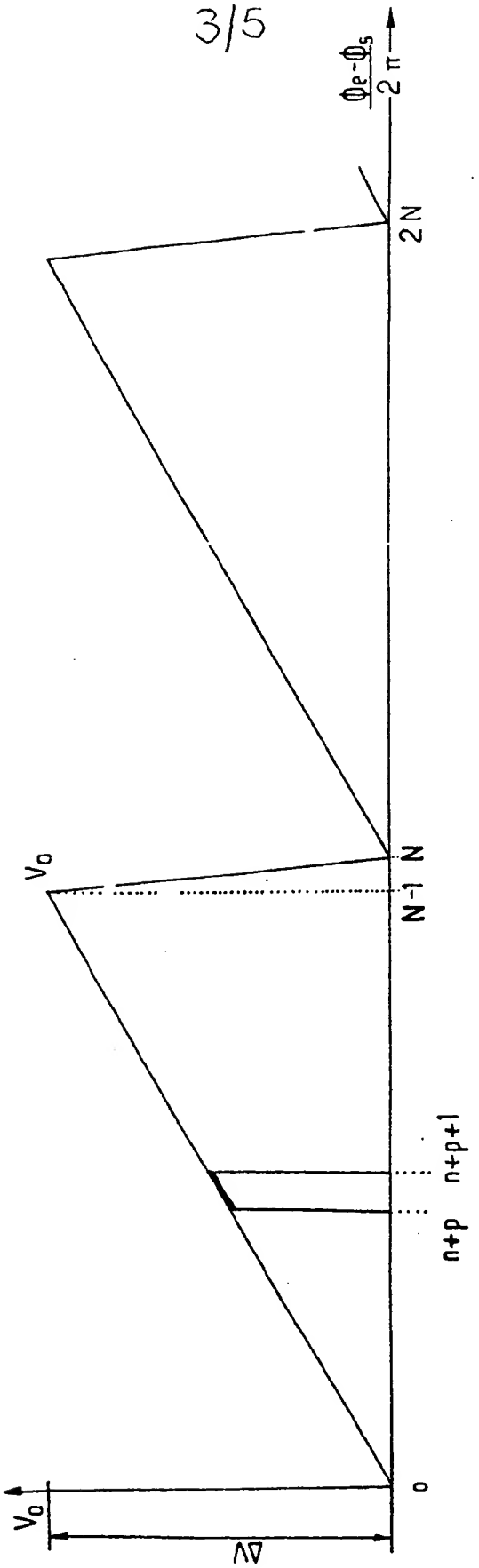


FIG 3

FIG 4

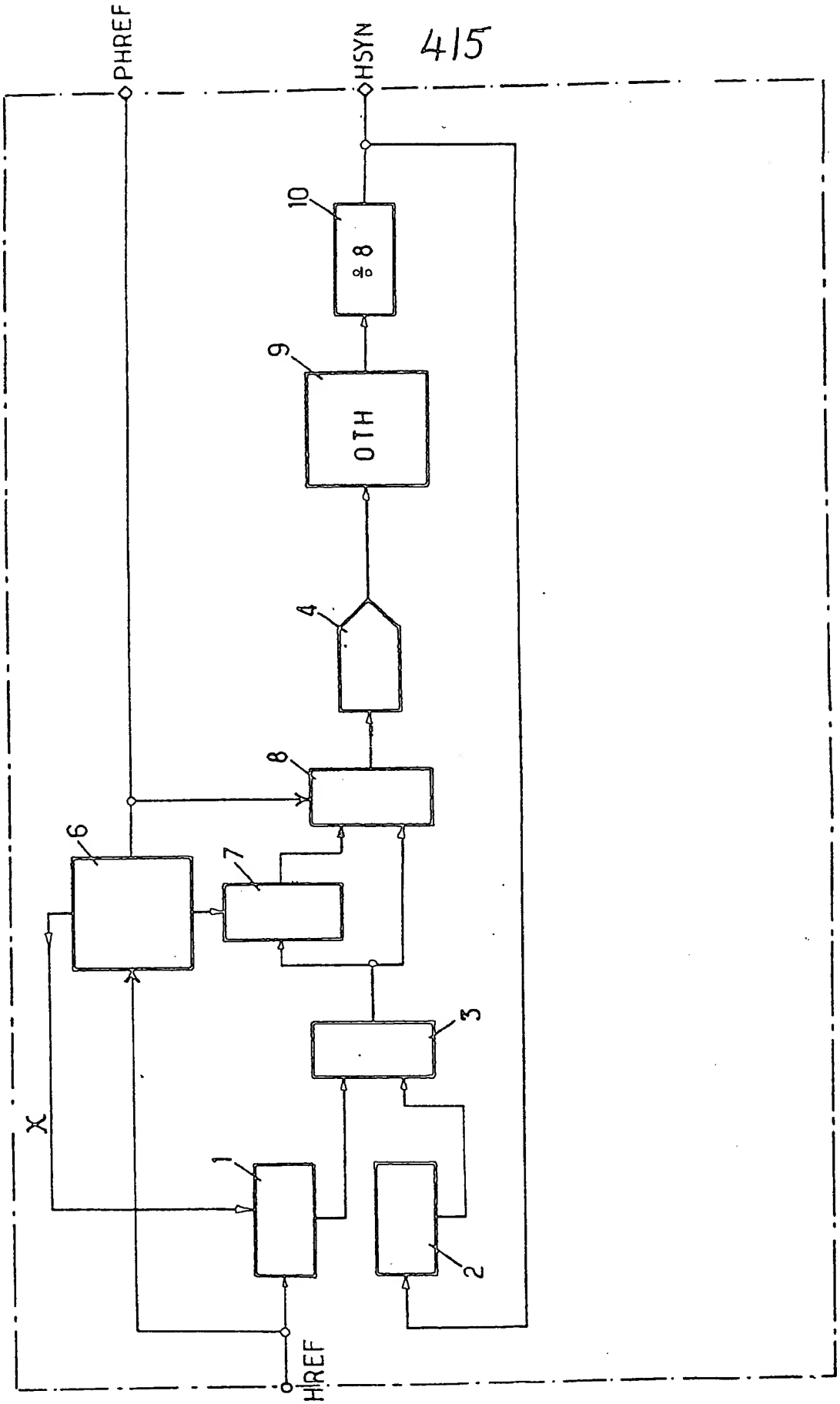
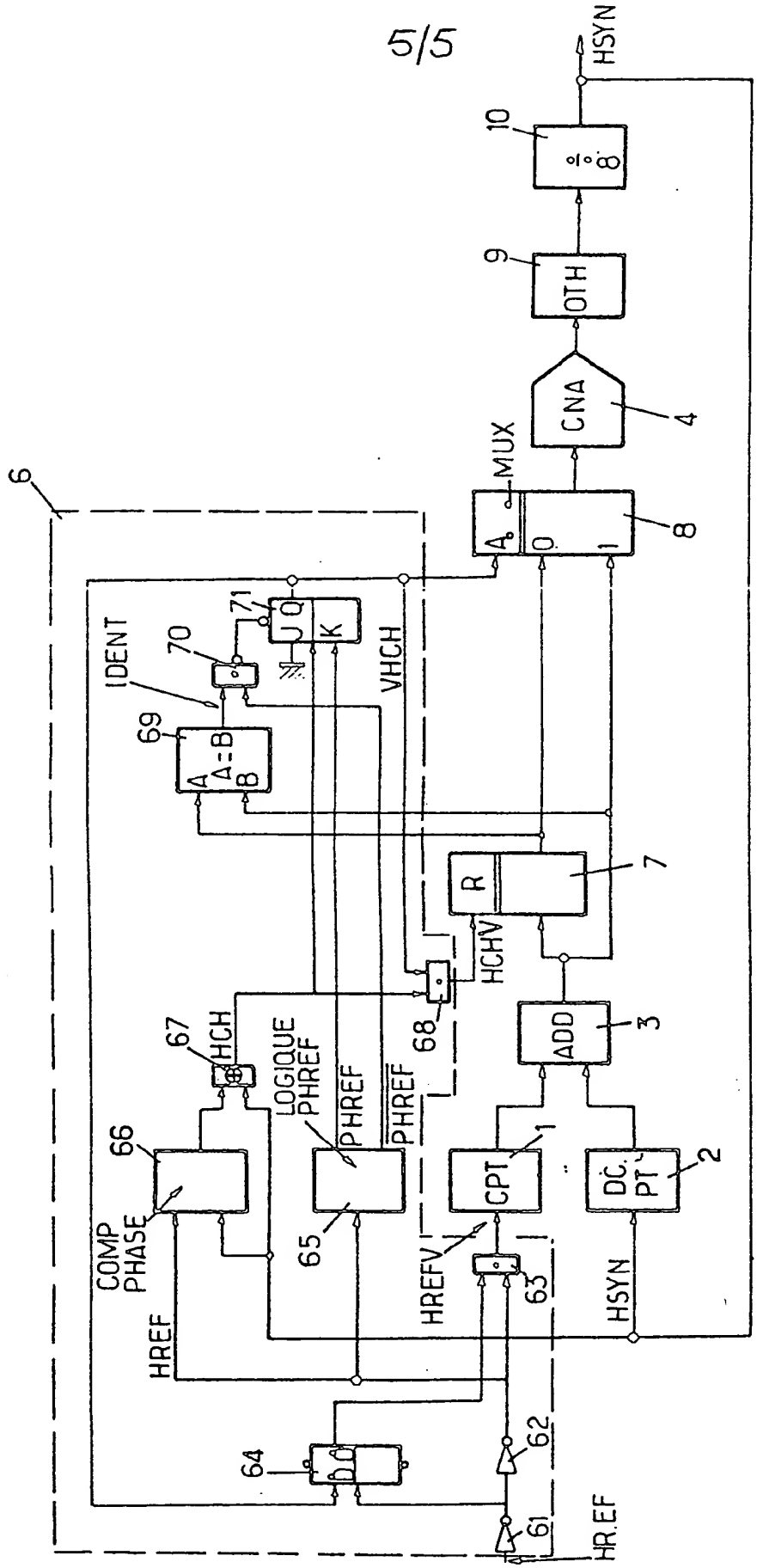


FIG 5



SPECIFICATION

Digital device for clock signal synchronization

The present invention relates to a digital device for synchronising a clocking signal of local frequency f_e on a clock signal of incident frequency f_e, comprising a phase lock loop comprising first means adapted to discriminate, digitally, the phase difference between the signals of frequencies f_e and f_s, second means adapted to convert said difference into a voltage, the mean value of said voltage being obtained over a period of the reference signal f_e and controlling an oscillator furnishing the signal at the locked frequency f_s.

Such a device is used as time base of a connecting network.

A connecting network must be capable of receiving digital signals presenting a jitter going as far as a slip of several frames. Notice G 811 of the CCITT specifies the period separating two frame jumps at 70 days, which imposes a precision of the oscillators higher than 10^{-11}, which imposes synchronization of the connecting networks.

The synchronization interface is a signal at 2048 kHz whose long-term relative precision is 10^{-11}. This interface aims at synchronizing the local master clock of the network on the reference clock.

It is an object of the present invention to correct the phase of the local clock of the network by synchronizing it on the master clock f_e furnished by the synchronization interface.

A device of the type depicted hereinabove is described in U.S. Patent No. 3 989 931.

In addition, European Patent Application 0 025 217 teaches storing, from a device of this type, the phase difference between the incident and locked clock signals in order, in the event of loss of the incident synchronization rhythm f_e, to maintain the frequency correction existing before the loss of rhythm.

However, phase detection is effected by means of a second oscillator adapted to count the pulses in a determined gate. According to this process of detection, it is not possible continuously to measure a phase difference and, in addition, phase storage is directed to the mean phase error and not to the instantaneous error. Finally, it is a cyclical storage at predetermined instants.

Consequently, it is an object of the present invention to overcome these drawbacks, to propose a device giving higher performance, to allow fortuitous storage, for example in the event of loss of a clock pulse.

To this end, the present invention relates to a device of the type depicted hereinabove, characterized in that it further comprises means for storing the instantaneous phase difference issuing from said first means, the stored phase difference being applied to the input of said second means as soon as a pulse of the incident clock signal f_e disappears, and third means adapted to compare the instantaneous phase difference issuing from said first means and the stored phase difference issuing from said storage means, said third means being adapted to allow take up of the instantaneous phase difference only after and identity of said phase differences.

In a preferred embodiment of the device of the invention, said third means are arranged to generate a phase selection signal at the input of a multiplexer, said selection signal further making it possible to block the advance of an upcounter of said first means, to accelerate the search of the identity of said phases.

The invention will be more readily understood on reading the following description with reference to the accompanying drawings, in which:

Figure 1 is a schematic representation of the phase loop according to the invention.

Figure 2 is a representation of the state of the upcounter and downcounter of Figure 1.

Figure 3 is the characteristic curve of the digital phase discriminator of Figure 1 in locked mode.

Figure 4 is an embodiment of Figure 1 with storage of the phase-shift.

Figure 5 is a detailed view of the loop of Figure 4.

Referring now to the drawings, and firstly to Figure 1, the signal f_e of the reference clock is applied to the input of an upcounter 1 with N states, whilst signal f_s of the local clock is applied to the input of a downcounter 2 likewise with N states. The upcounter 1 and downcounter 2 respectively furnish a signal indicative of the state of phase of the signals of frequencies f_e and f_s at the input of an adder 3 likewise with N states. In this way, the adder 3 can make the difference between the phases of these two signals.

The state of the upcounter 1 and downcounter 2 is illustrated in Figure 2. Thus state n corresponds, for example, to a clock period f_e. At the following period, the upcounter 1 will be in state n+1. Inversely, the downcounter 2 being in state p, it passes to state p—1 at the following period. If the two clocks f_e and f_s are in different states of phase, i.e. offset in time, the adder 3 is in a state n+p when the upcounter 1 is in state n and the downcounter 2 in state p. Let us assume, as in Figure 2, that the local clock f_s is delayed; in that case, when the upcounter 1 passes to state n+1, the downcounter 2 is still in state p, therefore the adder 3 is in state n+p+1.

As soon as the downcounter 2 advances in the following period, it passes to state p—1 then returns the adder 3 to state n+p. As the clock signals f_e and f_s have the same period but are simply phase-shifted, the states n+p+1 and n+p of the adder 3 are periodically reproduced during a period of the reference clock signal f_e. If the reference period corresponds to 2π and the phase shift to θ_r, then the mean state at the output of the adder 3 over a reference period is equal to

$$(n+p+1)\frac{\theta_r}{2\pi}+(n+p)\frac{2\pi-\theta_r}{2\pi}=n+p+\frac{\theta_r}{2\pi}$$

The signal indicative of the state of the adder 3 is applied to the input of a digital/analog converter 4, which enables a voltage V_M proportional to the phase difference to be obtained. This voltage V_M is used for controlling an oscillator 5 at controlled frequency.

The mean voltage V_M, over a period of the reference signal, varies proportionally to θ_r since the adder 3 presents a mean state equal to

$$n+p+\frac{\theta_r}{2\pi}.$$

The oscillator 5 comprises, at the input, an RC filter (not shown in Figure 1) with time constant of appropriate magnitude, which enables this mean V_M to be obtained. In this way, the mean value V_M continuously varies proportionally to the phase difference θ_r between the two clocks. This allows an exact setting on the instantaneous reference frequency of clock f_e. In practice, the RC filter may be eliminated, this function being performed by the input circuits of the frequency-controlled oscillator 5.

At the output of the oscillator 5, the frequency f_s phase locked on frequency f_e is obtained.

In this way, the phase discriminator according to the invention comprises the upcounter 1 and downcounter 2, the adder 3 and the digital/analog converter 4; it is characterized by the ratio K1 between the maximum variation of direct voltage V_a obtained at the output of the converter 4 and the maximum phase variation acceptable at the input of the discriminator. This maximum phase variation is proportional to the number of states of the upcounter 1 and downcounter 2 and of the adder 3. The coefficient K1 is written:

$$K1=\frac{\Delta Vmax}{2\pi(N-1)}$$

The phase error measured is a periodic function of the true phase error with an amplitude of $2\pi(N-1)$.

Figure 3 illustrates the characteristic curve of the phase error; it is a continuous saw-tooth curve of period $2\pi N$.

Figure 4 shows the phase loop of Figure 1 in greater detail and in a preferred embodiment. In the event of loss of incident rhythm f_e, it is advantageous to store the earlier phase error in order to maintain the frequency correction existing before the loss of rhythm.

To this end, a register 7 is provided which stores the signal issuing from the adder 3, indicative of the phase difference between the local rhythm f_s and the incident rhythm f_e. The incident rhythm f_e is received by the up-counter 1 with N states as well as by a device 6 for detecting loss of reference clock. The device 6 detects a loss of clock signal f_e as soon as a clock pulse is lacking and furnishes a signal, at the input of the register 7, indicative of the reception of the input signal f_e and allowing the charge of the output signal of the adder 3 at the input of a multiplexer 8. In addition, the detection device 6 furnishes at its output a signal indicative of the loss the reference clock which is applied to the multiplexer 8. The multiplexer 8 then validates the phase stored by the register 7 at the instant of loss. During the loss of the reference clock signal f_e, the upcounter 1 is blocked and the output of the adder 3 varies at the rhythm of the downcounter 2 which receives the local clock signal H S Y N. The multiplexer 8 then transmits the last result of the phase shift furnished by the adder 3 and contained in the register 7. This signal indicative of the phase shift is applied, from the output of the multiplexer 8 and, whether or not there is loss of reference clock f_e, to the input of a digital/analog converter 4.

As soon as the reference clock f_e reappears, the phase validation furnished by the upcounter 1 is delayed up to the instant when the signal obtained at the output of the adder 3 is identical to the stored phase shift furnished by the register 7. During this time, the upcounter 1 remains blocked, in order to describe the cycle more quickly, by application of a signal X furnished by the device 6.

The digital/analog converter 4 furnishes at its output a voltage proportional to the phase difference and which controls a frequency controlled oscillator 9. The mean value of this voltage, obtained by an RC filter (not shown). disposed at the input of the oscillator 9, over a period of the reference signal f_e, varies the phase shift directly proportionally to θ_r. The oscillator 9 is thermally controlled and makes it possible to generate a signal If 1.4 V peak to peak at 16 384 kHz, for example, with a stability of some 10^{-8} in the range of 0°C to 50°C.

A divider (10) divides by 8 the frequency furnished by the oscillator 9 and furnishes at its output a signal H S Y N. The frequency control voltage is included between −3.5 V and +3.5 V and causes a frequency variation of about a hundred hertz per volt on frequency 16 384 kHz.

Figure 5 shows in detail the detection device 6 of Figure 4 in stored mode. It is composed of various elements. The incoming reference signal H R E F is applied to the input of a monostable multivibrator 65 after a double inversion, in the embodiment described, by means of two inverters 61 and 62 in series, which therefore restore the signal H R E F at the input of the monostable multivibrator 65. This monostable multivibrator 65 furnishes at its output Q a signal P H R E F and its complement on its output $\overline{Q}$. The signal P H R E F is a signal "one" as soon as a pulse is lacking in the input signal H R E F and it is a signal "zero" after one second of continuous presence of input signal H R E F. It is indicative of the loss of phase of the reference signal. A phase comparator

66 receives at its input the signal H R E F issuing from the inverter 62 as well as the signal H S Y N obtained at the output of the divider-by-eight (10), at the output of the digital synchronization device. The phase comparator 66 makes it possible to choose the phase of the charge clock H C H which is either in phase or in phase opposition with H S Y N, in order to avoid any risk due to the changes of state of the adder 3.

This choice is made by an exclusive OR circuit 67, which receives on the one hand the result of the comparison of the phase comparator 66 and on the other hand the signal H S Y N. The signal H C H issuing from the circuit 67 is applied to the input of an AND circuit 68 which validates the signal H C H by a charge clock validation signal V H C H which will be introduced subsequently. The signal HC HV issuing from the circuit 68 is applied to the storage register 7 as charge signal. Moreover, the incoming reference clock signal H R E F, after inversion into $\overline{\text{H R E F}}$ by means of the inverter 61, is applied to the input of a flip flop 64 whose input D receives the same signal V H C H. The output Q of this flip flop 64 furnishes a signal which validates the incoming reference clock signal H R E F at the input of the AND circuit 63. The outgoing signal H R E F V of the circuit 63 is applied to the input of the upcounter 1. The downcounter 2 receives the synchronization clock signal H S Y N obtained at the output of the synchronization device of the invention and applies its state signal to the input of the addition circuit 3. In the same manner as for the earlier Figures, the addition circuit 3 effects an addition of the states of the upcounter 1 and downcounter 2 and furnishes its results to the input of the multiplexer 8 and the storage register 7.

This magnitude indicative of the stored phase difference, issuing from the register 7, is applied to the input of a comparison circuit 69 which also receives the current phase difference issuing from the addition circuit 3. Thus the comparison circuit 69 may compare the state of the new phase with the last state of phase. The result of the comparison is applied to the input of a NAND circuit 70. This circuit 70 also receives the signal $\overline{\text{P H R E F}}$ indicative of the reference clock signal issuing from the circuit 65. The result of the circuit 70 is applied to the input of a flip flop 71 whose input J is connected to ground, the input K receives the signal P H R E F indicative of the loss of the reference clock. The charge clock signal H C H issuing from the exclusive OR circuit 67 is also applied to the clock input of the flip flop 71.

On the output Q of the flip flop 71 is obtained the signal V H C H which is thus synchronized by the signal H C H. This signal V H C H, indicative of the normal operational (locked), or stored mode, is therefore applied to the input of the AND circuit 68 as well as to the input of the flip flop 64. This signal V H C H is also applied to the input A_0 of the multiplexer 8 in which it controls the choice of the phase difference applied to the converter 4. In fact, when the signal V H C H is equal to 0, the multiplexer 8 switches towards the output the input 0, i.e. the stored phase issuing from the register 7 and when the signal V H C H is equal to 1, the multiplexer 8 switches towards the output the input 1, i.e. the current phase leaving the addition circuit 3.

Thus, in summary:—

in normal operation: P H R E F=0 and V H C H=1

in the event of loss, P H R E F=1 whilst signal V H C H passes to zero with synchronization by H C H to avoid distorting a pulse H C H V and the phase difference stored in the register 7 is switched by the multiplexer 8 towards the converter 4.

in the event of restart, when P H R E F passes from 1 to 0, in order to avoid a jump between the stored state and the state at the output of the addition circuit 3, the output of the circuit 3 at the input of the multiplexer 8 (and a new charge in the register) is validated only after the identity of the stored state (in the register 7) and of the state at the output of the addition circuit 3, has been assured (by means of the comparator 69).

The signal V H C H also allows multiplexing synchronized with the signal H C H by means of multiplexer 8.

The signal V H C H also blocks the upcounter 1 after synchronization by the signal H R E F at circuit 63 level as long as the comparator 69 displays a non-identity between the stored value and the value issuing from the addition circuit 3.

This accelerates identity search by blocking the upcounter 1 due to the AND circuit 63 when the signal V H C H is equal to zero.

In fact, whilst P H R E F is equal to 1, the downcounter 2 continues to count down. After restart of the incident clock, the signal P H R E F passes to zero and if the frequency H R E F were very close to the locked frequency H S Y N, the upcounter 1 and downcounter 2 would effect their cycle at the same speed and the signal IDENT issuing from the comparator 69 would be late in appearing. Consequently, the blocking of the upcounter 1 by means of the signal V H C H resynchronized by H R E F is particularly advantageous.

In the same manner as in locked mode, the signal issuing from the multiplexer 8 is applied to the input of an analog converter 4.

The digital/analog converter 4 furnishes at the output a voltage proportional to the stored phase difference which controls at the output a frequency controlled oscillator 9. The oscillator 9 is thermally controlled and makes it possible to generate a signal of 1.4 V peak to peak at 16 384 kHz, for example, with a stability of some 10^{-8} in the range of 0°C to 50°C.

A divider (10) divides by eight the frequency furnished by the oscillator 9 and furnishes at the output a signal H S Y N. The frequency control voltage is between −3.5 V and +3.5 V and brings about a frequency variation of about a hundred hertz per volt on frequency 16 384 kHz.

Such a device is particularly advantageous for synchronizing the clock signals of a connecting

network with respect to a reference clock transmitted by a synchronization interface.

Claims

1. Digital device for synchronizing a clock signal of local frequency f_o on a clock signal of incident frequency f_e, comprising a phase lock loop comprising first means adapted to discriminate, digitally, the phase difference between the signals of frequencies f_e and f_o, second means adapted to convert said difference into a voltage, the mean value of said voltage being obtained over a period of the reference signal f_e and controlling an oscillator furnishing the signal at the locked frequency f_o, characterized in that it further comprises means for storing the instantaneous phase difference issuing from said first means, the stored phase difference being applied to the input of said second means as soon as a pulse of the incident clock signal f_e disappears, and third means adapted to compare the instantaneous phase difference issuing from said first means and the stored phase difference issuing from said storage means, said third means being adapted to allow take up of the instantaneous phase difference only after an identity of said phase differences.

2. The device of Claim 1, characterized in that said third means are adapted to generate a phase selection signal at the input of a multiplexer, said selection signal further making it possible to block the advance of an upcounter of said first means, to accelerate the search for the identity of said phases.

3. Digital device for clock signal synchronization, substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

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